CLAIMS

1. An apparatus comprising:

a clock generator configured to generate a first clock signal and a second clock signal, wherein the timing relationship between the first and second clock signals is arbitrary and wherein the first and second clock signals are individually adjustable; and

a phase detector coupled to receive the first and second clock signals, the phase detector generating a skip signal by integrating the first clock signal, wherein the skip signal indicates whether the first clock signal is ahead of the second clock signal.

2. An apparatus as recited in claim 1 wherein the value of the skip signal is based on the phase difference between the first clock signal and the second clock signal.

3. An apparatus as recited in claim 1 wherein the skip signal has a first value if the first clock signal is ahead of the second clock signal and the skip signal has a second value if the second clock signal is ahead of the first clock signal.

4. An apparatus as recited in claim 1 wherein the phase detector generates a skip signal by integrating the first clock signal over one half of a clock cycle.

5. An apparatus as recited in claim 1 further including an inverter coupled to an output of the phase detector.

6. An apparatus as recited in claim 1 wherein the phase detector is a quadrature phase detector.

7. An apparatus as recited in claim 1 wherein the first and second clock signals are calibrated individually.

8. An apparatus as recited in claim 1 wherein the skip signal indicates whether a load pulse should be sampled.

9. A method comprising:

receiving a first clock signal and a second clock signal;

shifting the phase of the first clock signal by 90 degrees using a quadrature phase detector; and

generating a skip signal indicating whether a load pulse should be sampled, wherein the value of the skip signal is based on the phase difference between the first clock and the second clock.

10. A method as recited in claim 9 wherein the skip signal has a first value if the first clock signal is ahead of the second clock signal and the skip signal has a second value if the second clock signal is ahead of the first clock signal.

11. A method as recited in claim 9 wherein the shifting the phase of the first clock by 90 degrees includes integrating the first clock signal.

12. A method as recited in claim 9 wherein the shifting the phase of the first clock by 90 degrees includes integrating the first clock signal over one half of a clock cycle.

13. A method as recited in claim 9 wherein the first and second clock signals are individually adjustable.

14. A memory system comprising:

a memory storage device;

a data bus coupled to the memory storage device;

a clock generator configured to generate a first clock signal and a second clock signal, wherein the timing relationship between the first and second clock signals is arbitrary; and

a memory controller coupled to the data bus, the memory controller including a phase detector coupled to receive the first and second clock signals, the phase detector generating a skip signal based on the phase difference between the first clock signal and the second clock signal.

15. A memory system as recited in claim 14 wherein the phase detector generates a skip signal by integrating the first clock signal over one half of a clock cycle.

16. A memory system as recited in claim 14 wherein the first and second clocks are individually adjustable.

17. A memory system as recited in claim 14 wherein the phase detector is a quadrature phase detector.

18. A memory system as recited in claim 14 wherein the first and second clock signals are calibrated individually.

19. A memory system as recited in claim 14 wherein the skip signal indicates whether the load pulse should be sampled.

20. A memory system as recited in claim 14 wherein the skip signal has a first value if the first clock signal is ahead of the second clock signal, and the skip signal has a second value if the second clock signal is ahead of the first clock signal.